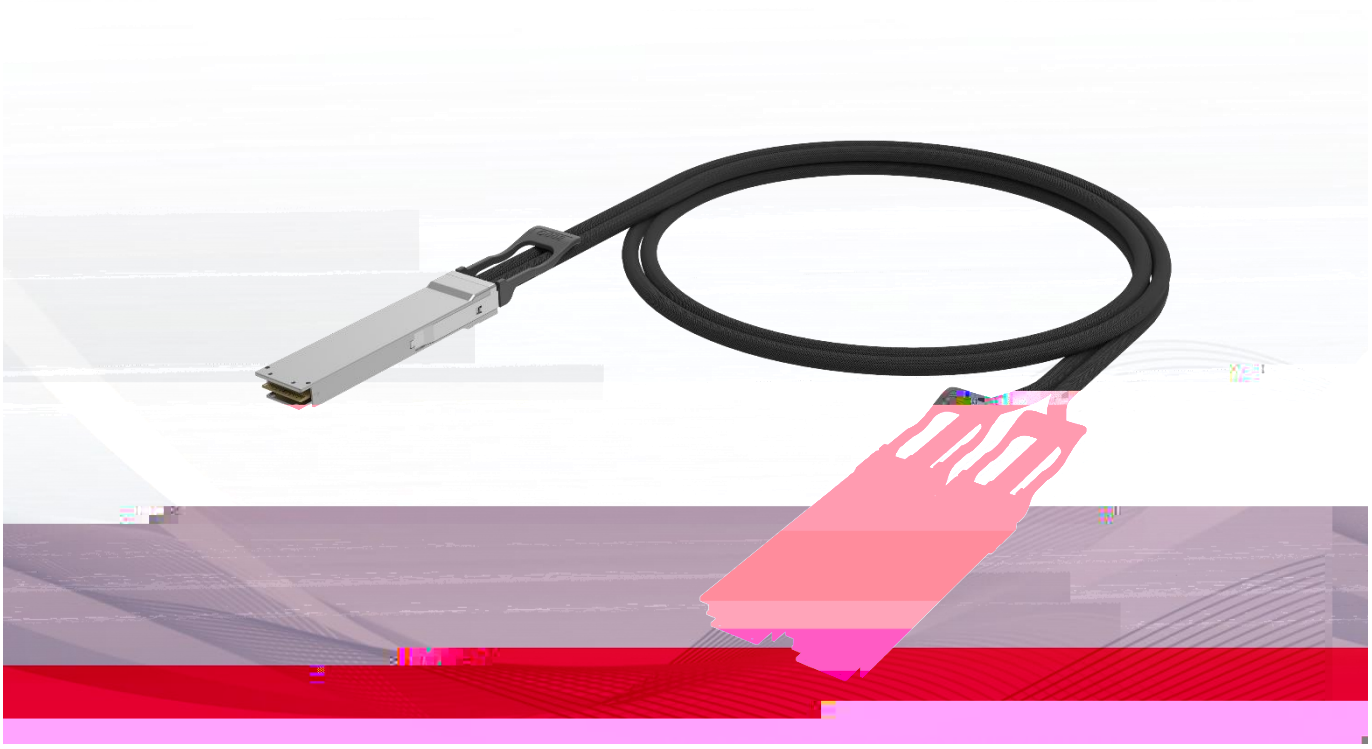

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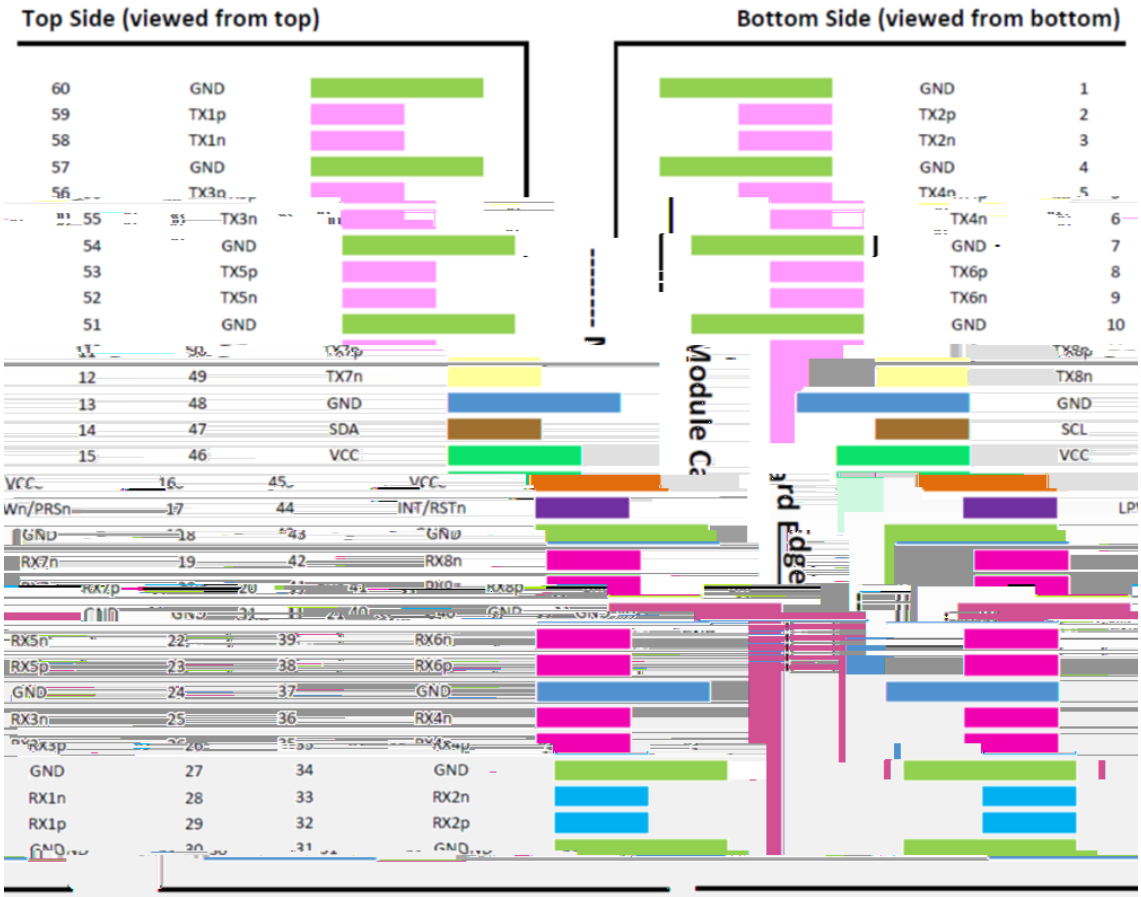
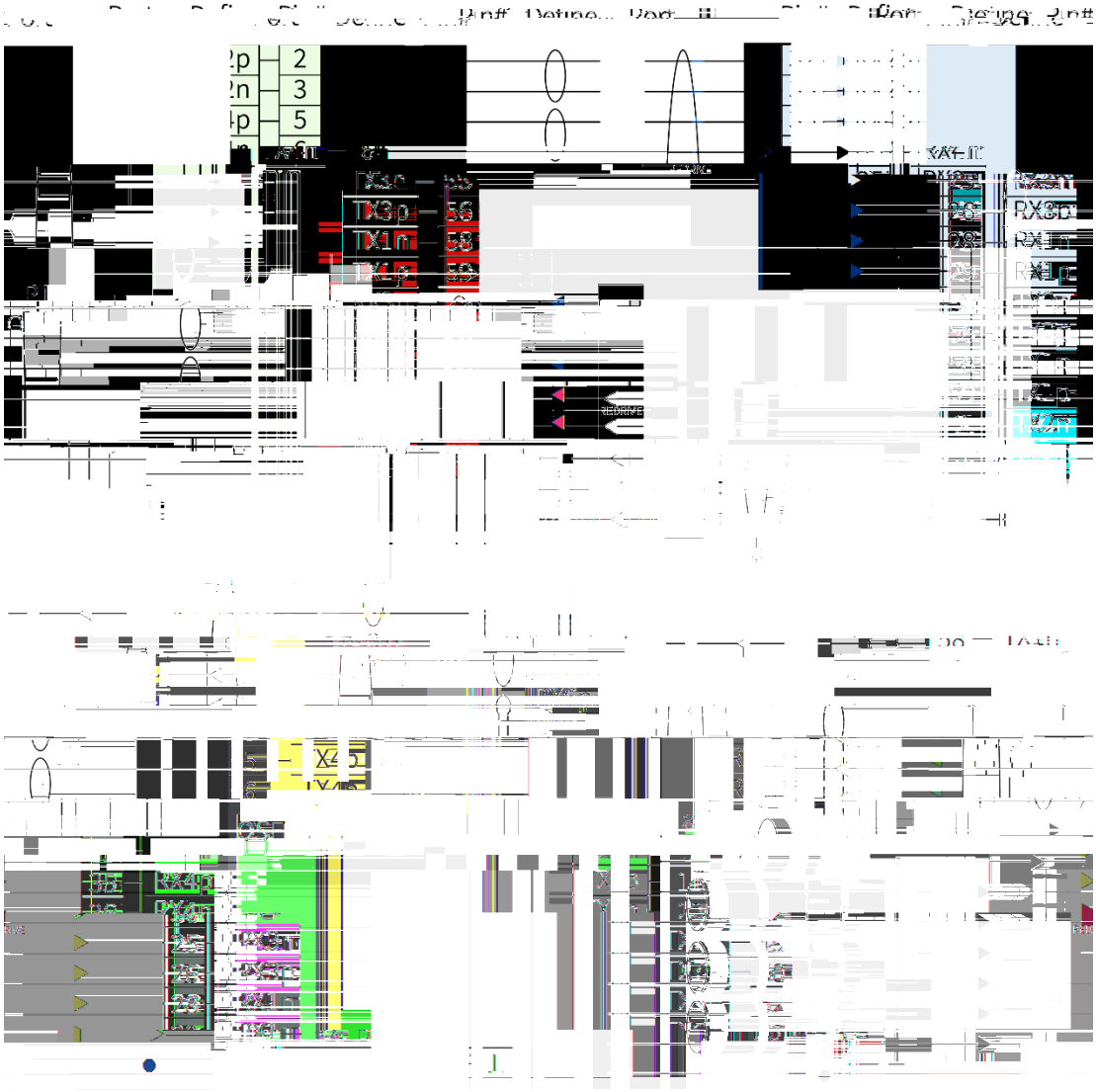
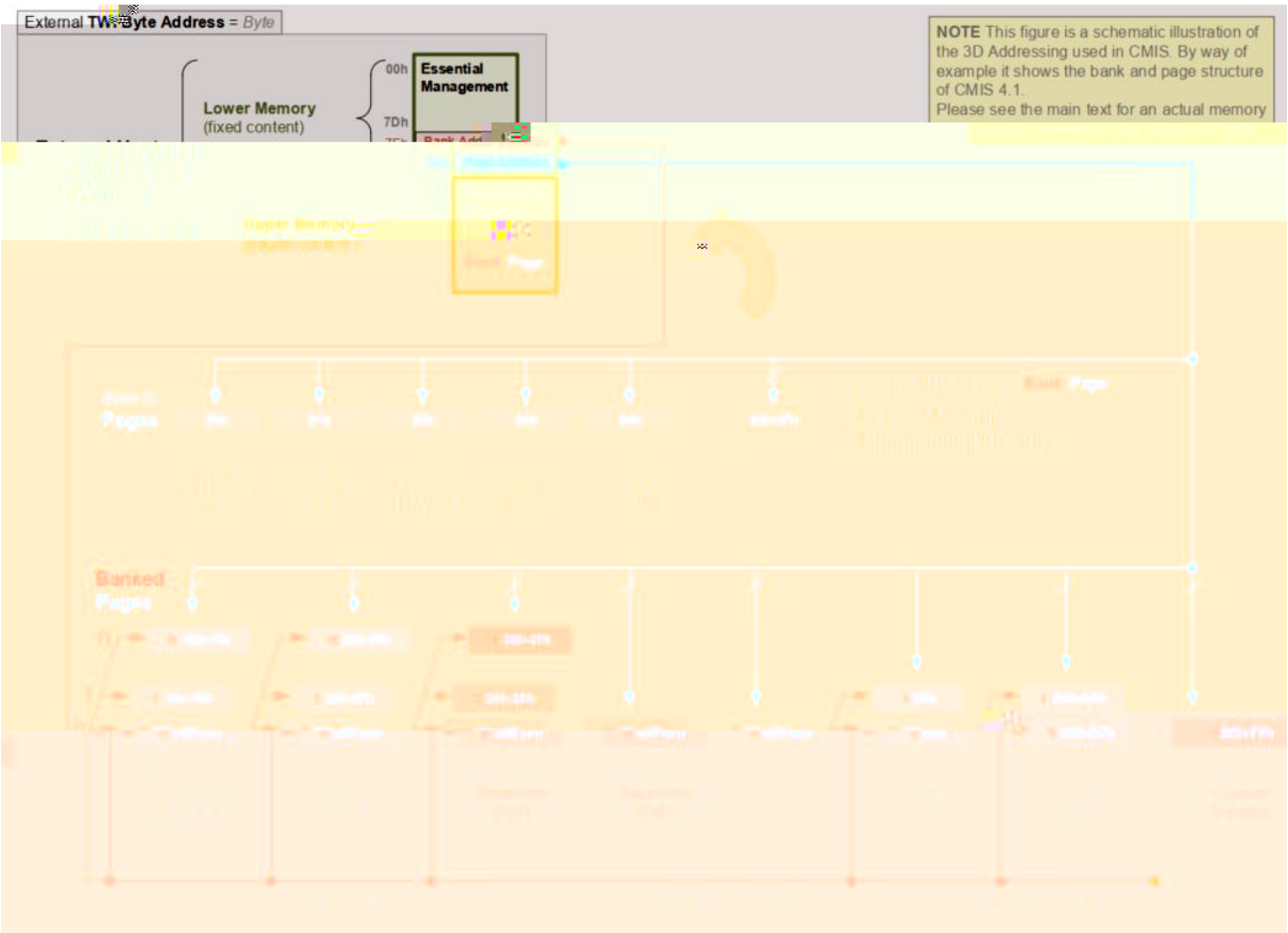

Top Side (viewed from top)
Bottom Side (viewed from bottom)
60 GND
59 TX1p
58 TX1n
57 GND
55 TX3n
54 GND
53 TX5p
52 TX5n
51 GND
12 49 TX7n
13 48 GND
14 47 SDA
15 46 VCC
17 44 INT/RSTn
19 42 RX8n
22 39 RX6n
23 38 RX6p
24 37 GND
25 36 RX4n
27 34 GND
28 33 RX2n
29 32 RX2p
GND 1
TX2p 2
TX2n 3
GND 4
TX4n 6
GND 7
TX6p 8
TX6n 9
GND 10
TX8n
GND
SCL
VCC

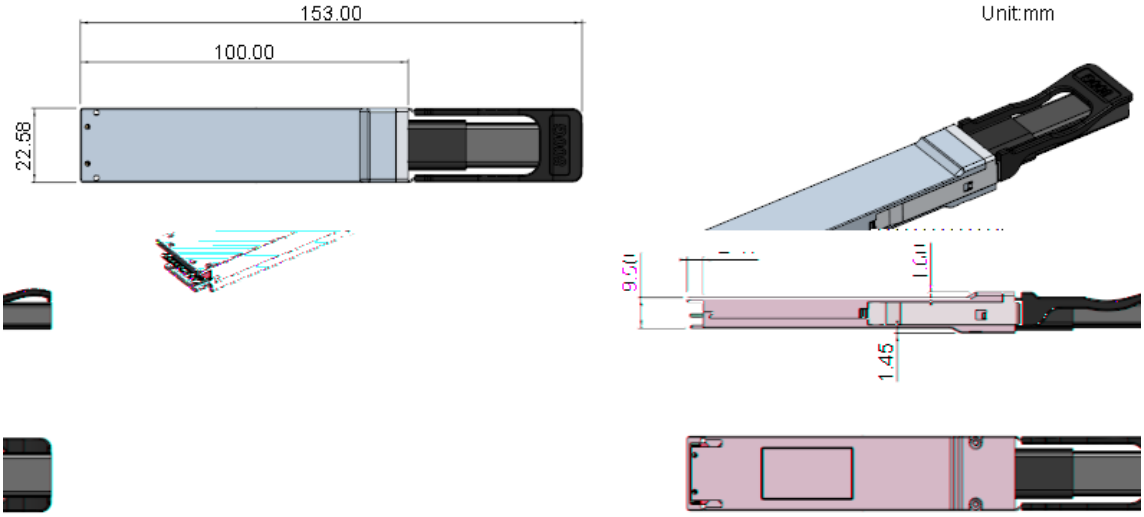
WIRING TABLE




External TWI Byte Address = Byte
Lower Memory
(fixed content)
00h
Essential
Management
7Dh
NOTE This figure is a schematic illustration of the 3D Addressing used in CMIS. By way of example it shows the bank and page structure of CMIS 4.1.
Please see the main text for an actual memory

■ [illegible]

■


153.00
100.00
22.58
Unit:mm
9.50
1.60
1.45