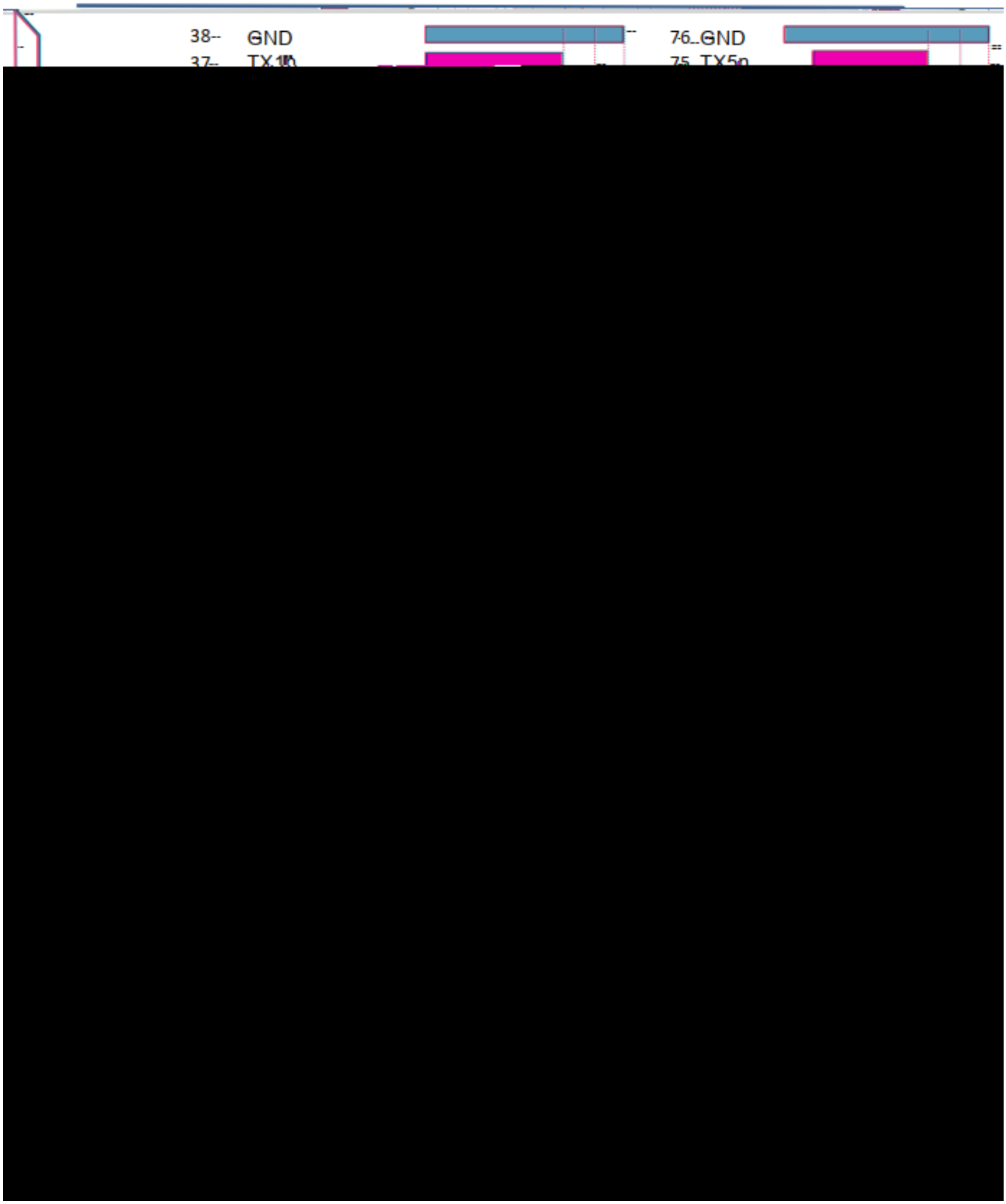
- Data Center & Networking Equipment
- Servers/Storage Devices
- High Performance Computing (HPC)
- Switches/Routers
- Telecom Central Offices (CO)
- Test And Measurement Equipment

- Support 8x106.25G PAM4
- 800G To 4*200G Data Rate
- 3.3V Power Supply
- Hot Pluggable
- Excellent SI Performance
- RoHS Compliance
- Simplifies The Patching And Offers A Cost-Effective Way For Short Links

- Compliant with QSFP-DD MSA Rev 4.1
- Compliant QSFP-DD-Hardware-Rev7.0
- Compliant with OSFP MSA Rev 4.1
- Compliant with IEEE 802.3ck
- Compliant with IEEE 802.3cd
- I2C for EEPROM communication
- Compliant with CMIS 5.0

G

Top PCB viewed from top



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13		GND	Ground	1B	1
14	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
15					

52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1:

QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP- DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector GND contact is rated for a steady state current of 500 mA.

Note 2:

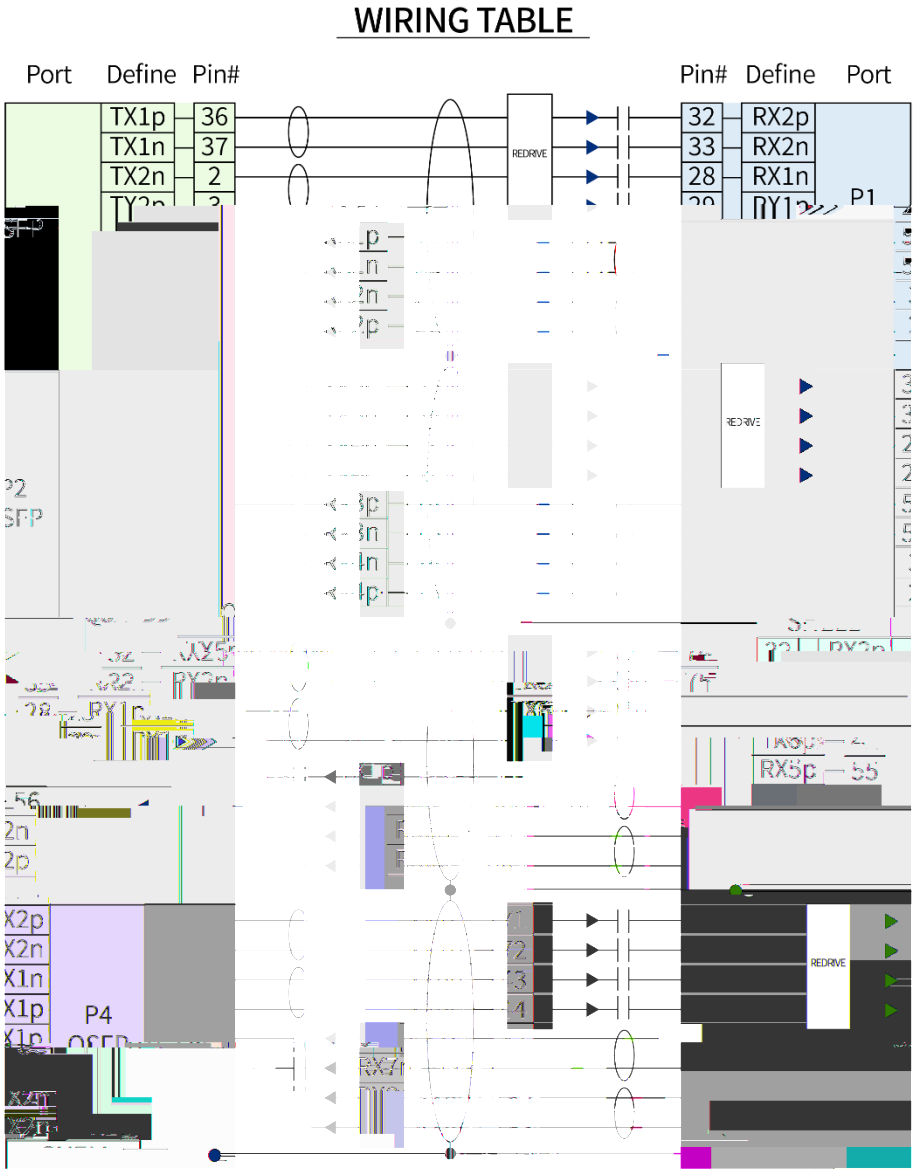
VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector(see MSA specification). For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 2000 mA

will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B
Note 5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.
Note 6: For host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	TX2p	Transmitter Data Non-Inverted	3	
3	CML-I	TX2n	Transmitter Data Inverted	3	
4		GND	Ground	1	
5	CML-I	TX4p	Transmitter Data Non-Inverted	3	
6	CML-I	TX4n	Transmitter Data Inverted	3	
7		GND	Ground	1	
8	CML-I	TX6p	Transmitter Data Non-Inverted	3	
9	CML-I	TX6n	Transmitter Data Inverted	3	
10		GND	Ground	1	
11	CML-I	TX8p	Transmitter Data Non-Inverted	3	
12	CML-I	TX8n	Transmitter Data Inverted	3	
13		GND	Ground	1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	1
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3	2
18		GND	Ground	1	
19	CML-O	RX7n	Receiver Data Inverted	3	
20	CML-O	RX7p	Receiver Data Non-Inverted	3	
21		GND	Ground	1	
22	CML-O	RX5n	Receiver Data Inverted	3	
23	CML-O	RX5p	Receiver Data Non-Inverted	3	
24		GND	Ground	1	
25	CML-O	RX3n	Receiver Data Inverted	3	

26	CML-O	RX3p	Receiver Data Non-Inverted	3	
27		GND	Ground	1	
28	CML-O	RX1n	Receiver Data Inverted	3	
29	CML-O	RX1p	Receiver Data Non-Inverted	3	
30		GND	Ground	1	
31		GND	Ground	1	
32	CML-O	RX2p	Receiver Data Non-Inverted	3	
33	CML-O	RX2n	Receiver Data Inverted	3	
34		GND	Ground	1	
35	CML-O	RX4p	Receiver Data Non-Inverted	3	
36	CML-O	RX4n	Receiver Data Inverted	3	
37		GND	Ground	1	
38	CML-O	RX6p	Receiver Data Non-Inverted	3	
39	CML-O	RX6n	Receiver Data Inverted	3	
40		GND	Ground	1	
41	CML-O	RX8p	Receiver Data Non-Inverted	3	
42	CML-O	RX8n	Receiver Data Inverted	3	
43		GND	Ground	1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3	2
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SDA	2-wire Serial interface data	3	1
48		GND	Ground	1	
49	CML-I	TX7n	Transmitter Data Inverted	3	
50		TX7p	Transmitter Data Non-Inverted	3	
51		GND	Ground	1	

M


WIRING TABLE
Port
Define
Pin#
Pin#
Define
Port
TX1p
TX1n
TX2n
36
37
2
32
33
28
RX2p
RX2n
RX1n
P1
REDRIVE
P4

G G G M

Lower Memory Overview

Page 00h Overview

G G G

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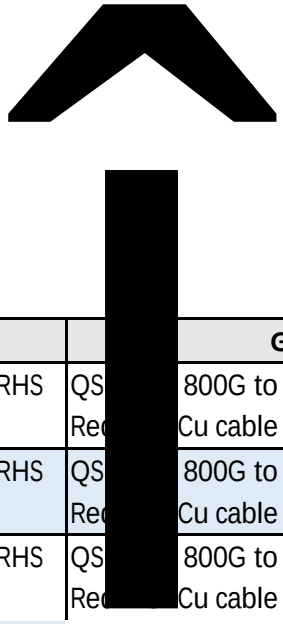

G		G		M
QSFP-DD800-4*OSFP-RHS 200G-ACC-3025	QS Rec	800G to 4* OSFP-RHS(2*100G) Active Cu cable , 30AWG-2.5M	±40	30
QSFP-DD800-4*OSFP-RHS 200G-ACC-3030	QS Rec	800G to 4* OSFP-RHS(2*100G) Active Cu cable , 30AWG-3.0M	±50	30
QSFP-DD800-4*OSFP-RHS 200G-ACC-3035	QS Rec	800G to 4* OSFP-RHS(2*100G) Active Cu cable , 30AWG-3.5M	±50	30
QSFP-DD800-4*OSFP-RHS				