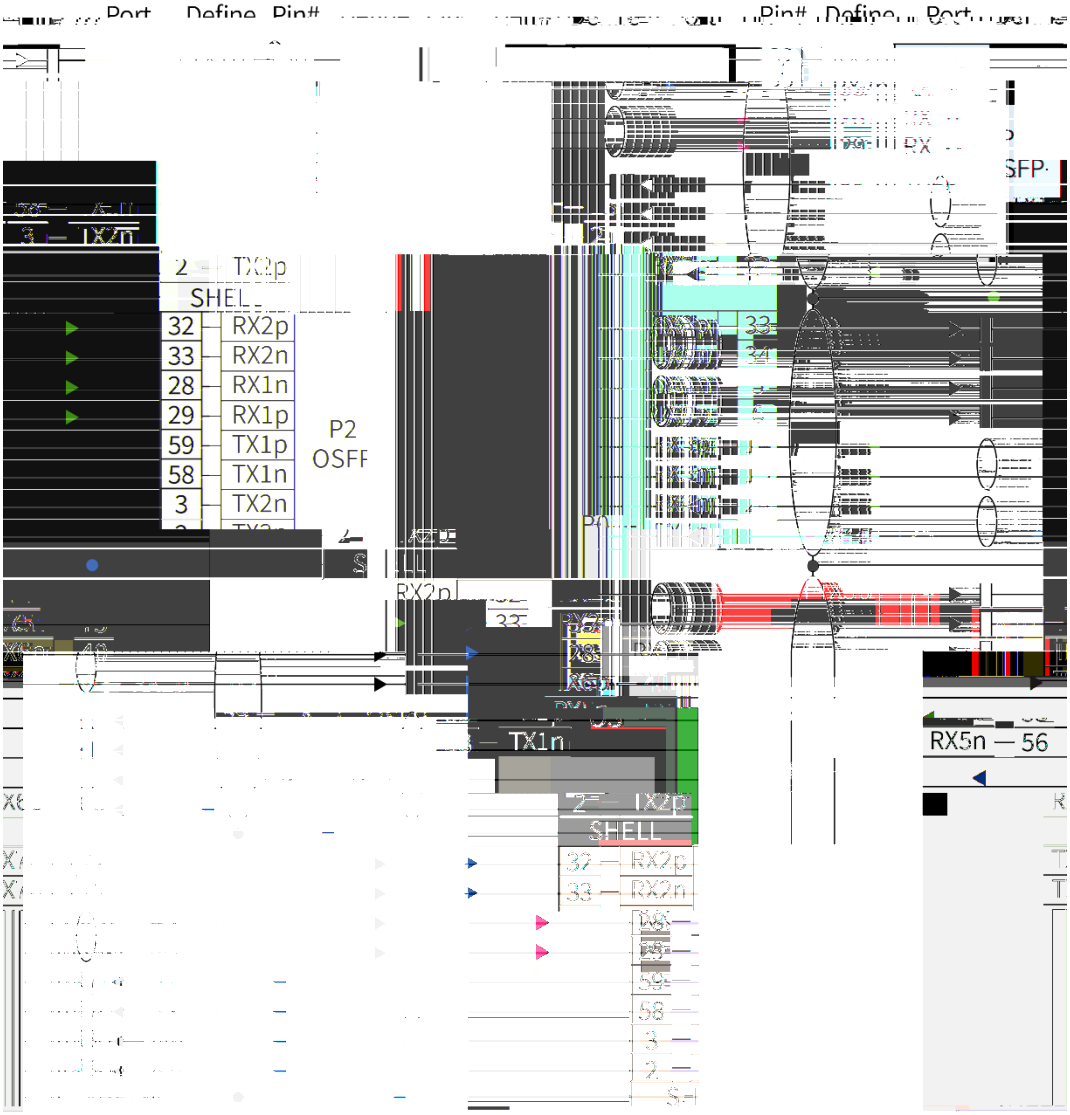
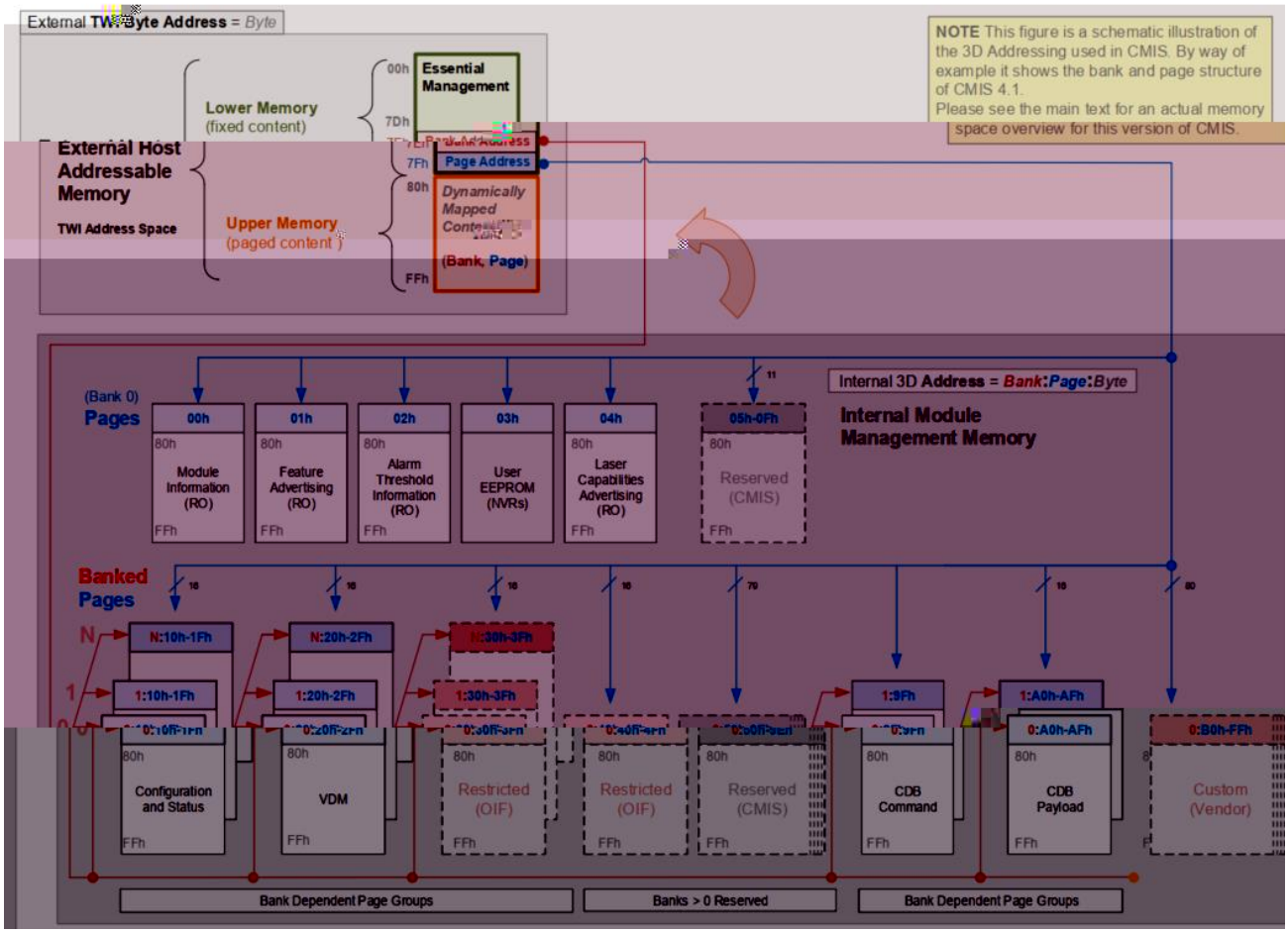
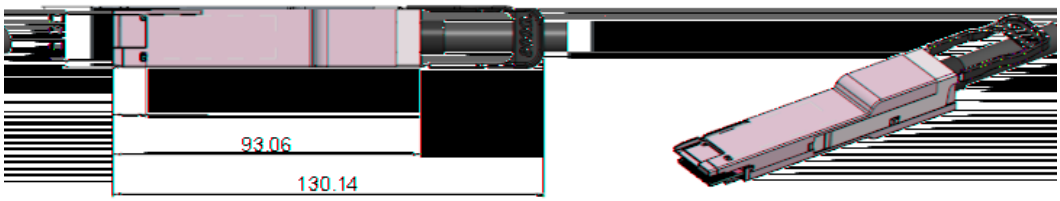
Top PCB viewed from top
Module Card Edge
38 GND
37 TX1n
36 TX1p
35 GND
34 TX3n
33 TX3p
32 GND
31 LPMode/TxDis
30 VCC1
29 VccTx
28 SCL
27 ModPrs
26 GND
25 RX5p
24 RX5n
23 GND
22 RX4p
21 RX4n
20 GND
76 GND
75 TX5n
74 TX5p
73 GND
72 TX7n
71 TX7p
70 GND
69 ePPS/Clock
68 VCC2
67 VccTx
66 VccRx
65 NC
64 GND
63 GND
62 RX2p
61 RX2n
58 GND
Bottom PCB viewed from bottom
19 GND
18 RX1n
17 RX1p
16 GND
15 RX3n
14 RX3p
13 GND
12 SDA
11 SCL
10 ModSelL
9 ResetL
8 VccRx
7 PWS3
6 PWS4
5 GND
4 TX4p
3 TX4n
2 GND
1 GND
57 GND
56 RX6n
55 RX6p
54 GND
53 RX7n
52 RX7p
51 GND
50 PWS2
49 PWS1
48 VccRx
47 PWS5
46 PWS6
45 GND
44 TX8p
43 TX8n
42 GND
41 TX6p
40 TX6n
39 GND
Classic
QSFP+/QSFP-DD Formfactor Pads
Additional
QSFP-DD Formfactor Pads

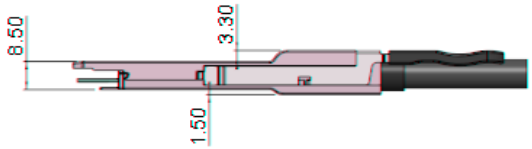
WIRING TABLE

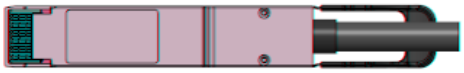



External TWI Byte Address = Byte
NOTE This figure is a schematic illustration of the 3D Addressing used in CMIS. By way of example it shows the bank and page structure of CMIS 4.1.
Please see the main text for an actual memory space overview for this version of CMIS.
External Host Addressable Memory
TWI Address Space
Lower Memory
(fixed content)
Upper Memory
(paged content)
00h
Essential Management
7Dh
Bank Address
7Fh
Page Address
80h
Dynamically Mapped Content
(Bank, Page)
FFh
Internal 3D Address = Bank:Page:Byte
Internal Module Management Memory
(Bank 0)
Pages
00h
Module Information (RO)
01h
Feature Advertising (RO)
02h
Alarm Threshold Information (RO)
03h
User EEPROM (NVRs)
04h
Laser Capabilities Advertising (RO)
05h-0Fh
Reserved (CMIS)
Banked Pages
N
1
N:10h-1Fh
1:10h-1Fh
N:20h-2Fh
1:20h-2Fh
N:30h-3Fh
1:30h-3Fh
1:9Fh
1:A0h-AFh
0:B0h-FFh
Configuration and Status
VDM
Restricted (OIF)
Restricted (OIF)
Reserved (CMIS)
CDB Command
CDB Payload
Custom (Vendor)
Bank Dependent Page Groups
Banks > 0 Reserved
Bank Dependent Page Groups

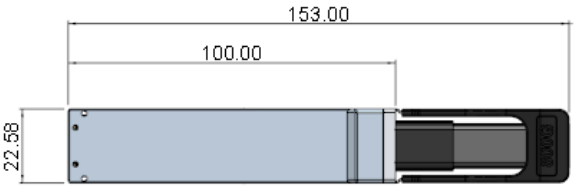
Unit:mm

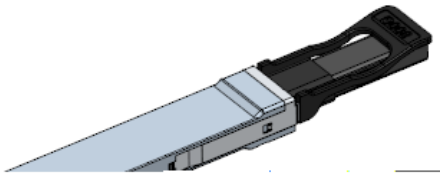


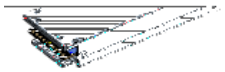


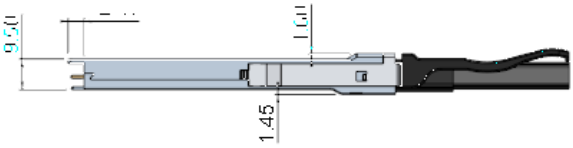


Unit:mm









Unit:mm