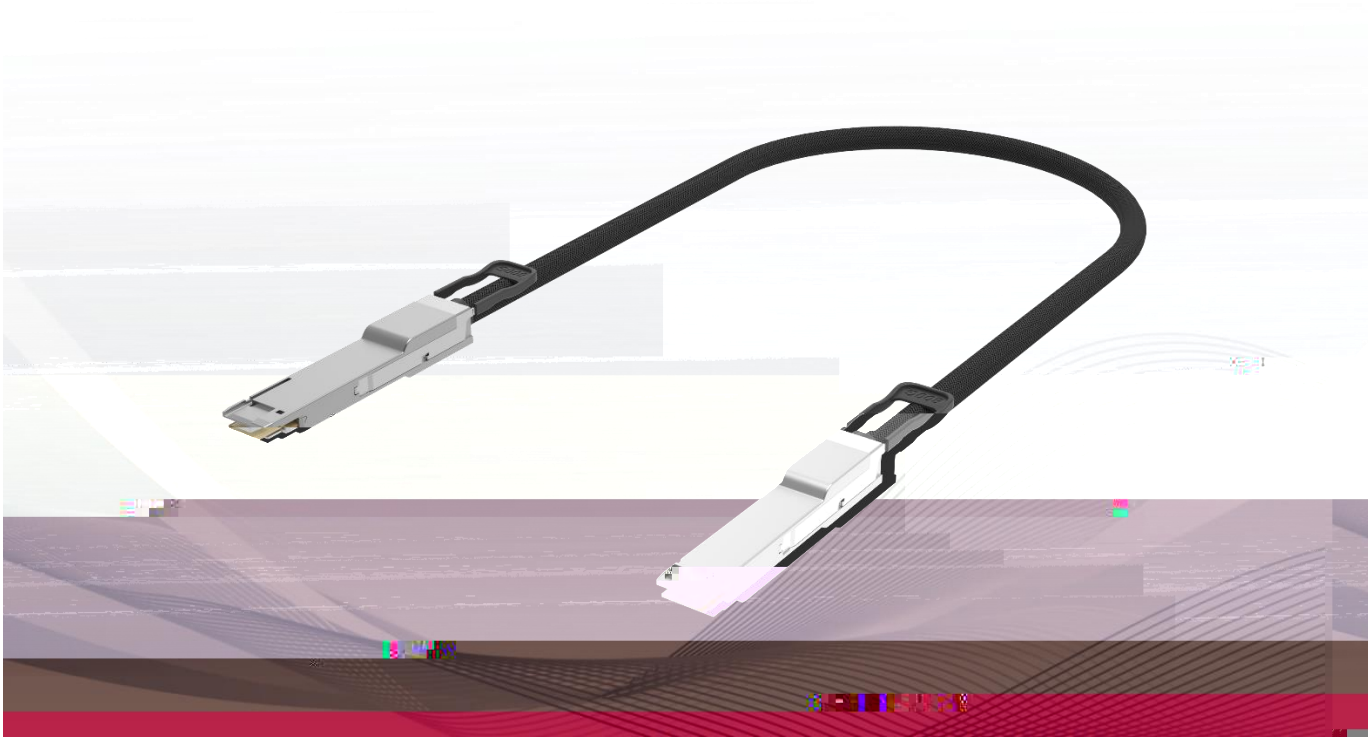
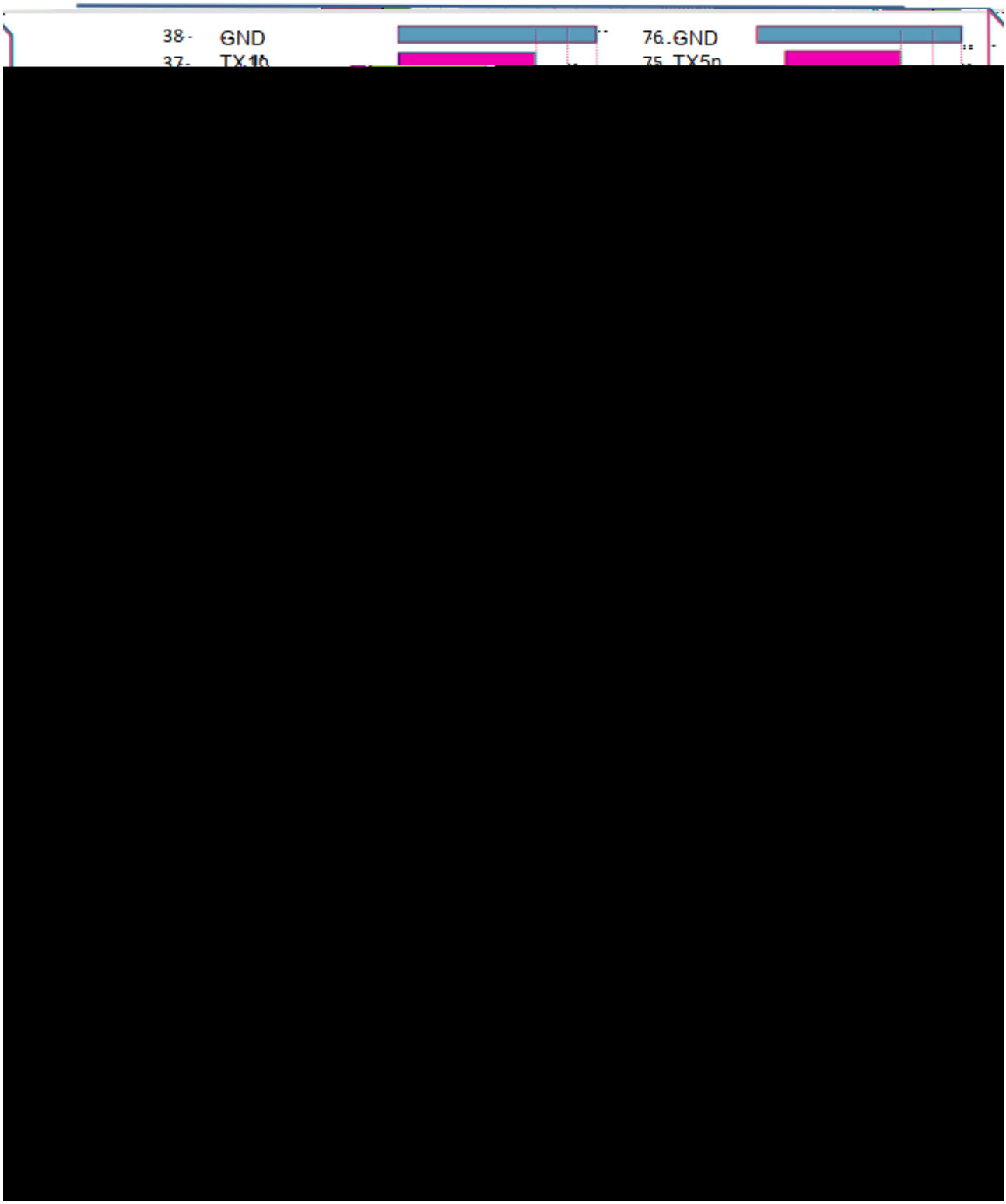
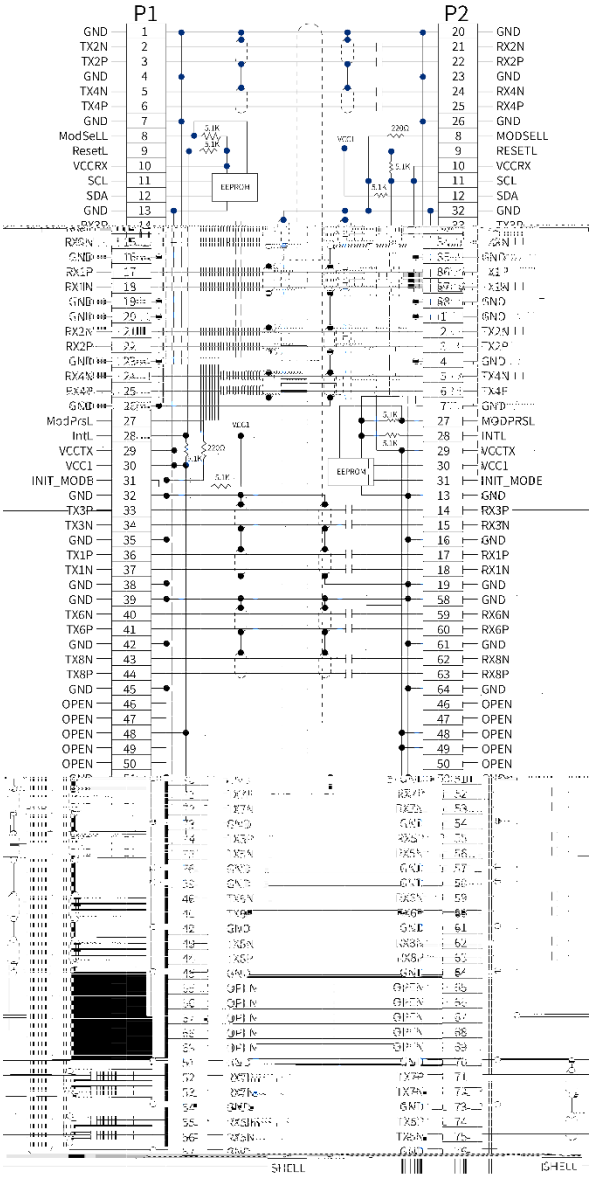


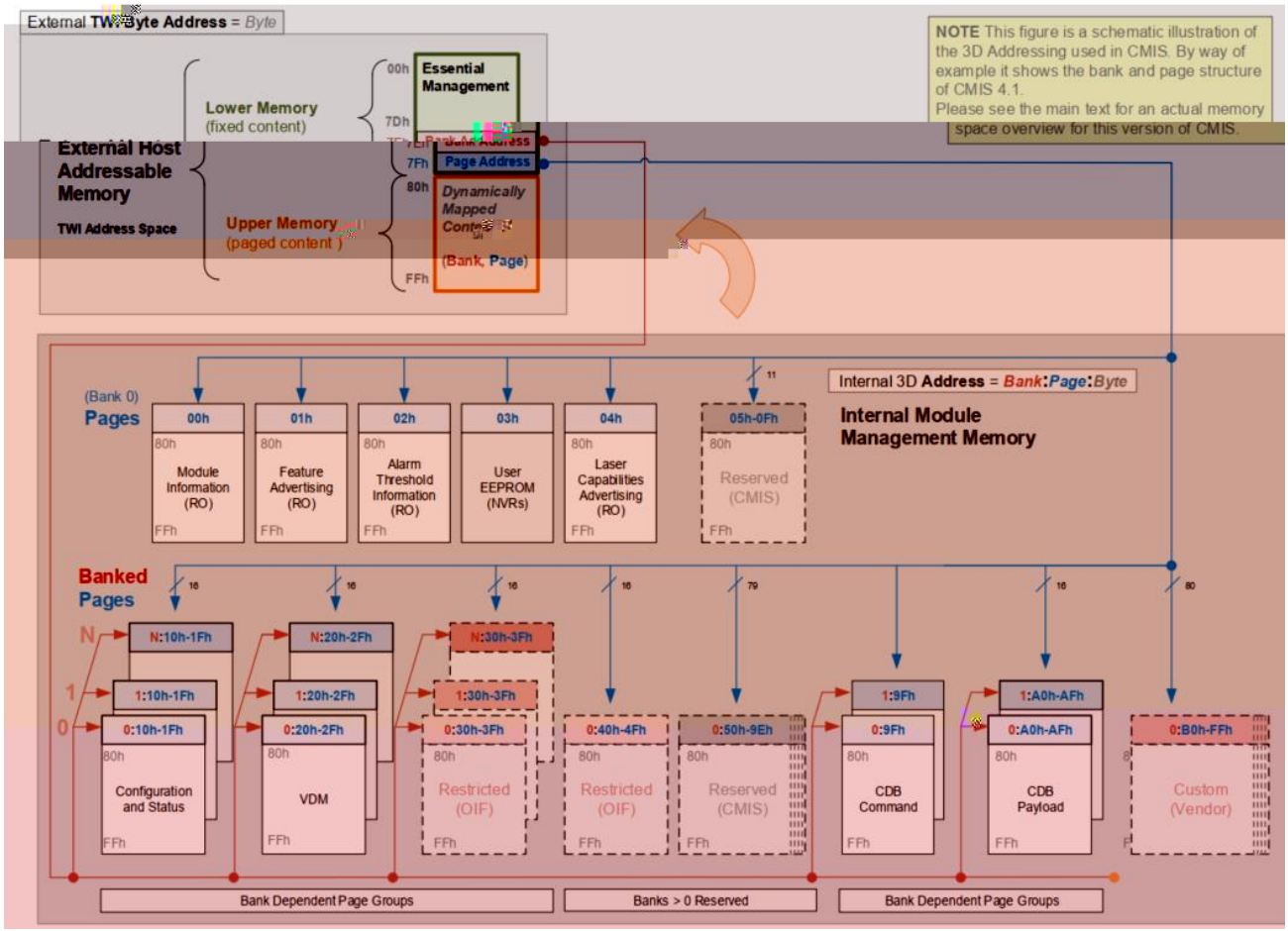
-
-
-

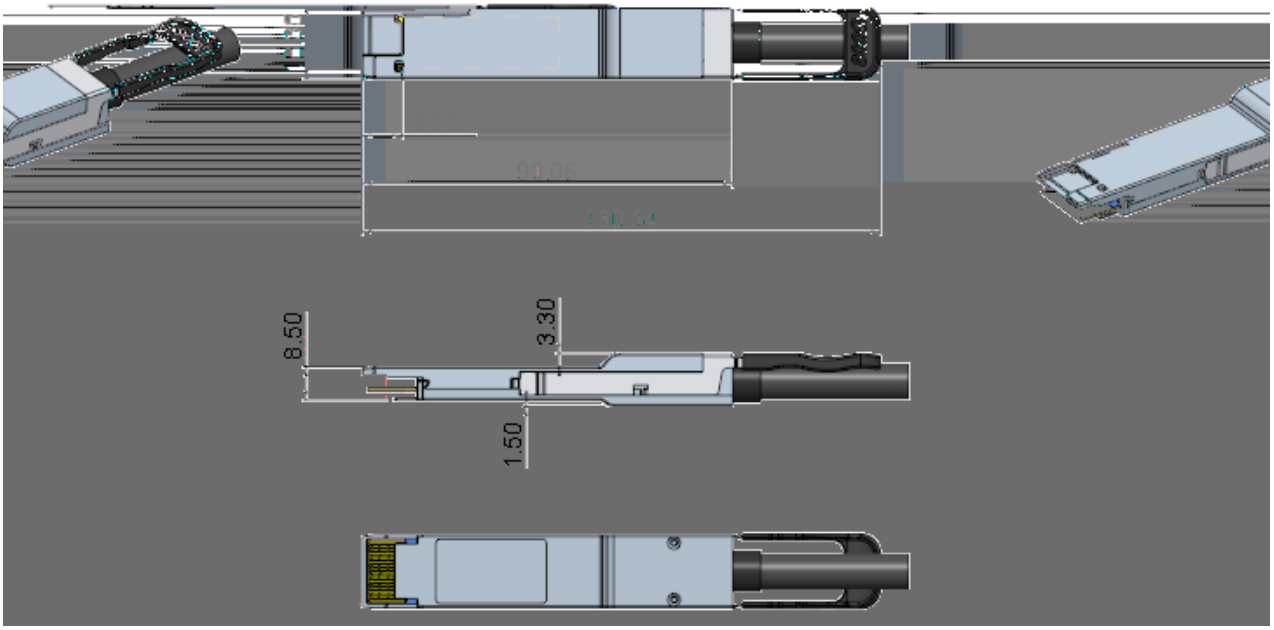
Top PCB viewed from top



WIRING TABLE




External TWI Byte Address = Byte
NOTE This figure is a schematic illustration of the 3D Addressing used in CMIS. By way of example it shows the bank and page structure of CMIS 4.1.
Please see the main text for an actual memory space overview for this version of CMIS.
External Host Addressable Memory
TWI Address Space
Lower Memory
(fixed content)
Upper Memory
(paged content)
00h
Essential Management
7Dh
Bank Address
7Fh
Page Address
80h
Dynamically Mapped Content
(Bank, Page)
FFh
Internal 3D Address = Bank:Page:Byte
Internal Module Management Memory
(Bank 0)
Pages
00h
Module Information (RO)
01h
Feature Advertising (RO)
02h
Alarm Threshold Information (RO)
03h
User EEPROM (NVRs)
04h
Laser Capabilities Advertising (RO)
05h-0Fh
Reserved (CMIS)
Banked Pages
N
1
0
N:10h-1Fh
1:10h-1Fh
0:10h-1Fh
Configuration and Status
N:20h-2Fh
1:20h-2Fh
0:20h-2Fh
VDM
N:30h-3Fh
1:30h-3Fh
0:30h-3Fh
Restricted (OIF)
0:40h-4Fh
Restricted (OIF)
0:50h-9Eh
Reserved (CMIS)
1:9Fh
0:9Fh
CDB Command
1:A0h-AFh
0:A0h-AFh
CDB Payload
0:B0h-FFh
Custom (Vendor)
Bank Dependent Page Groups
Banks > 0 Reserved
Bank Dependent Page Groups

■

Unit:mm