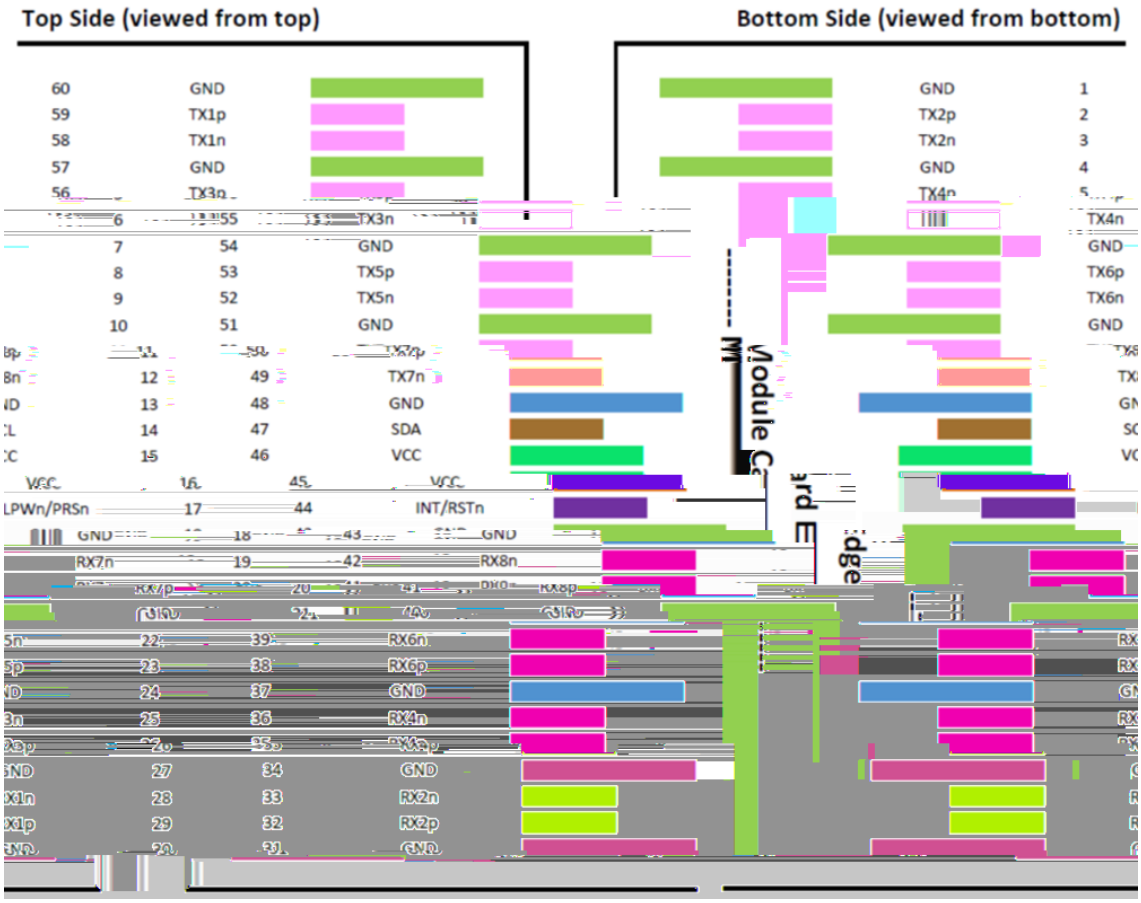
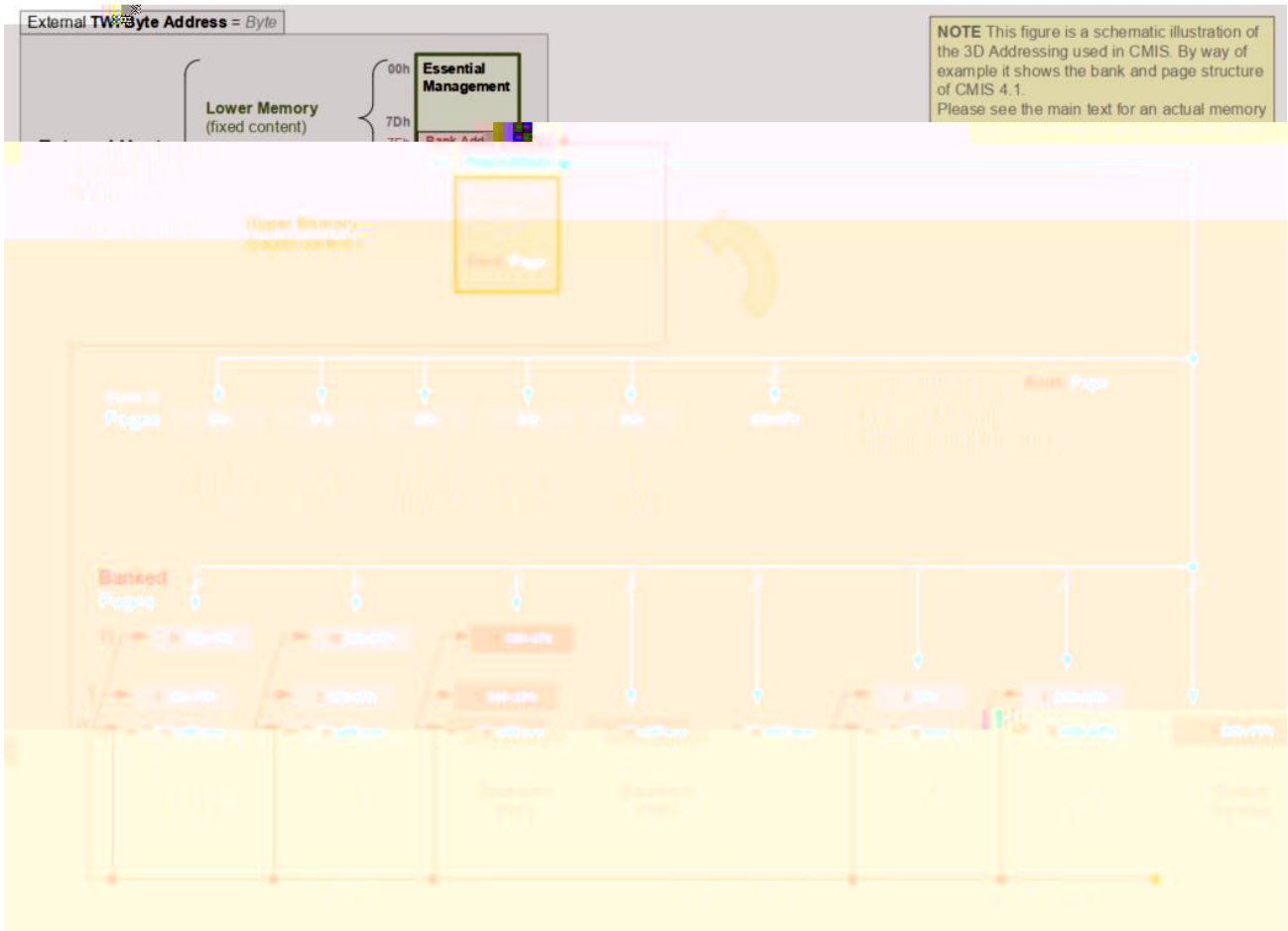
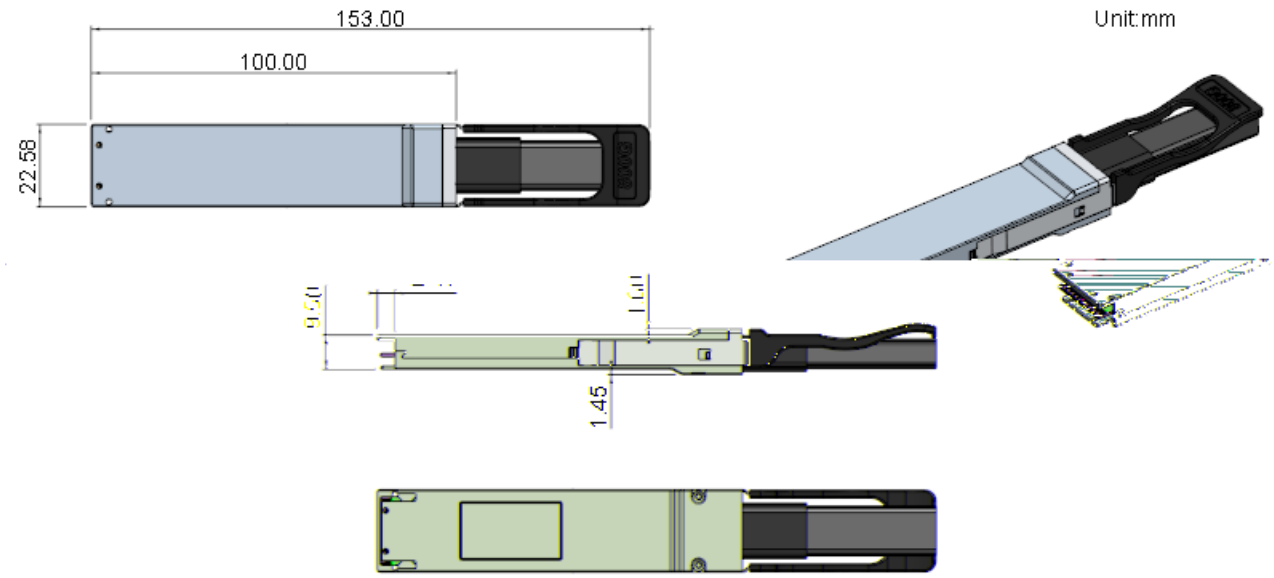
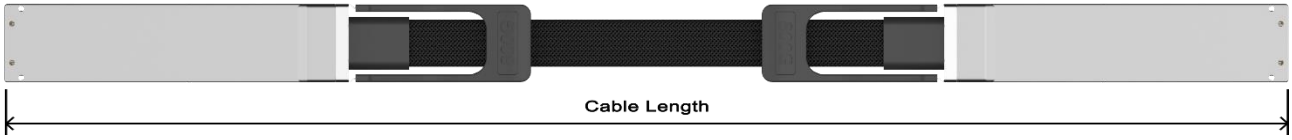

Top Side (viewed from top)
Bottom Side (viewed from bottom)
60 GND
59 TX1p
58 TX1n
57 GND
56 TX3p
55 TX3n
54 GND
53 TX5p
52 TX5n
51 GND
50 TX7p
49 TX7n
48 GND
47 SDA
46 VCC
45 VCC
44 INT/RSTn
43 GND
42 RX8n
41 RX8p
40 GND
39 RX6n
38 RX6p
37 GND
36 RX4n
35 RX4p
34 GND
33 RX2n
32 RX2p
31 GND
GND 1
TX2p 2
TX2n 3
GND 4
TX4p 5
TX4n 6
GND 7
TX6p 8
TX6n 9
GND 10
TX8p 11
TX8n 12
GND 13
SCL 14
SDA 15
VCC 16
VCC 17
GND 18
RX7n 19
RX7p 20
GND 21
RX5n 22
RX5p 23
GND 24
RX3n 25
RX3p 26
GND 27
RX1n 28
RX1p 29
GND 30


External TWI Byte Address = Byte
Lower Memory
(fixed content)
00h
7Dh
Essential Management
NOTE This figure is a schematic illustration of the 3D Addressing used in CMIS. By way of example it shows the bank and page structure of CMIS 4.1.
Please see the main text for an actual memory

■

■


153.00
100.00
22.58
Unit:mm
1.45

Unit:mm